

ATENEO DE MANILA UNIVERSITY
Loyola Schools
Generic Course Syllabus for 2nd Semester, School Year 2012-2013

Department	ECCE	School	SOSE
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Course No.	CE 150
Course Title	Computer Interfacing
No. of Units	3

Course Description:

This subject is designed to equip senior computer engineering students with the fundamental and hands-on concepts of sensors, computer interfacing and their applications. Aspects of buffering, address decoding, command decoding, timing and control needed in data transfers between various peripherals and a computer/microprocessor/controller are discussed. Design of interface using IC elements for commonly used peripherals, and interfacing different sensors to a computer, microprocessor or control unit are covered in this course.

Course Objective/s:

The course is "process-based" and aims to re-enforce the students' ability to look for and to discover solutions to computer interfacing projects and challenges in the professional world. The course aims to the extent practicable, students work on different aspects of computer interfacing, with the goal of developing "in-depth" insight on certain aspects, and a "helicopter view" of others.

Course Content:

- I. Introduction to Computer Interfacing
- II. Introduction to sensors
- III. Introduction to actuators
- IV. Arduino system
- V. Processing
- VI. Interfacing sensors
- VII. Controlling actuators
- VIII. Introduction to Project Management

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Department	ECCE	School	SOSE
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Course No.	CE 180
Course Title	PROGRAMMING LANGUAGES FOR ENGINEERS
No. of Units	3

Course Description:

This is an advanced digital design system course. This course covers hardware programming language – Verilog HDL. This course covers an introduction to Field Programmable Gate Array (FPGA).

Course Objective/s:

To have a hands-on knowledge of Verilog HDL and its applications.
To have a hands-on knowledge of FPGA and its applications.

Course Content:

- I. Introduction to FPGA
- II. Introduction to hardware programming languages.
- III. Introduction to Verilog HDL
- IV. Behavioral modeling using Verilog HDL
- V. Sequential processing using Verilog HDL
- VI. Verilog HDL synthesis
- VII. Verilog HDL Case Studies and Applications
- VIII. FPGA Applications

References:

Michael Ciletti, Modelling, Synthesis, and Rapid Prototyping with the Verilog HDL , Prentice Hall New Jersey 1999.
Andrew Rushton, Verilog for Logic Synthesis 2 nd Ed ., John Wiley & Sons 1999
Stephen Brown & Zvonko Vranesic, Fundamentals of Digital Logic with Verilog Design, McGraw-Hill International Edition, 2008.
M. Morris Mano, Digital Design Third Edition, Prentice Hall, Inc. 2002